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# Advanced Semiconductor Design through Specialized Printable Conductive Layer

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***Authors' contributions***

*This work was carried out in collaboration amongst the authors. All authors read, reviewed, and approved the final manuscript.*

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## ABSTRACT

Semiconductor package miniaturization and thinning have become of particular interest among semiconductor manufacturing industries, with each manufacturing company having specific approach and technical directions in providing unique solutions in their products. The paper provides a specialized design of manufacturing flow for semiconductor device through advanced fabrication method using stencil printing. The advanced process would significantly reduce the carrier thickness for the overall package height configuration of the device. The implementation of the specialized design and process would mitigate common assembly barriers and defects related in producing thin devices, hence, enabling cost-saving realization and manufacturing solution to package thinning and miniaturization with multiple input/output (I/O) requirements.

*Keywords: Assembly manufacturing; lead frame; substrate; stencil print; semiconductor.*

## 1. INTRODUCTION

Package thinning is one of the existing methods of maximizing the number of active components that could be incorporated in a single system, yet this approach also increases the thermal dissipation property of the semiconductor unit. Nowadays, competition among semiconductor

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companies exist for whichever offers possible thinnest architecture for surface mount technology (SMT) to reduce the direct material consumption which is positively correlated to the cost of the unit.

Existing approaches such as implementation of coreless substrate and etchable leadframes, qualification of thin silicon die through dicing before grinding, direct material such as die attach films (DAF), and upgrade of assembly equipment were known techniques among companies to lessen the package thickness however few offers new design and architecture of integrated circuit products that would cater the future of electronic packaging [1-4]. This paper discusses and provides a specialized design that offers thin package capability. The application is composed of new design and process for the carrier, revision in the assembly manufacturing flow of the device, and integration of new process brick such as carrier stencil and detaching process. The expected outcome would reduce the carrier thickness by 75 – 80% of the total substrate or leadframe thickness while enabling multiple input/output (I/O) integration in the design layout. The reduction in the thickness of the I/O also lowers the drain-to-source on-resistance ($RDS_{ON}$) of the package.

## 2. LITERATURE REVIEW AND PROCESS DESIGN SOLUTION

Realization of the specialized package is through the successive assembly flow as illustrated in Fig. 1. Note that process flow depends with the product and the technology [5-7]. The necessary wafer processing step to convert the wafer into individual dice is done in pre-assembly station including wafer taping, mounting and sawing. Printing process are responsible in producing the defined I/O layout on the stainless carrier through printing process of conductive adhesives then afterwards the individual silicon die is bonded to the “wet” conductive adhesives. The bonded units will be subjected to curing process to harden the adhesives and create a bondable I/O for wire interconnection between silicon die and I/O. The mold process is needed to encapsulate the wire bonded units by a mold material. stainless carrier will be detached from the molded units prior it is singulated or separated into individual device.

Printing of conductive material to the carrier can be through stencil process or similar process of dispensing. Example of adhesive material that can be used for printing: conductive epoxy, sintering paste, die attach film or newly formulated conductive paste suitable for this new process. A stainless carrier is recommended in this process due to the following: 1) the interfacial strength between adhesives and stainless carrier produces weak tensile and shear property when adhesive is cured; 2) weak interfaces create detaching process easy but enough adhesion to hold the I/O during wire bonding process. The coating of chromium on the surface of the glue prevents intermetallic formation for sintered glue yet the reinforced resins and polymers on the adhesives promotes temporary adhesion for the early process step of assembly. Shown in Fig. 2 is the cross-sectional view of the adhesive to the stainless carrier.

The interfacial strength of the glue to the stainless carrier should be higher to the force needed in forming the wire intermetallic. Shear strength both for wires and adhesives is the practical way of controlling the acceptable intermetallic strength. For adhesive, the recommended formula can be used, *L(adhesives) x W(adhesives) x 0.2 = Min. Shear requirement* where L(adhesives) refers to the length of the adhesives and W(adhesives) is for the width. Multiple design of printed pattern as shown in Fig. 3 is done to cater different I/O layout. Conventional design such as single array and advance design with 2 or more arrays are considered in the implementation of stainless carrier.

The stencil design is correlated with the actual thermal pad and I/O design. This will determine the actual footprint of the device when attach to the board or its actual application. In forming the stencil design, considerations are with the aperture and thickness of the stencil as shown in Fig. 4 which will determine the I/O layout and thickness. Current capability for the production of stencil is 50 µm thick. This may produce a thermal pad and I/O layer of 35 – 40 µm thickness since it collapses due to the outgassing of the adhesive upon curing.

The recommended assembly manufacturing flow is discussed in Fig. 5 shows the major process step to realize the specialized design of the semiconductor package. The conductive adhesive is applied to the stainless carrier using stencil process which is a known technique to dispense and spread the adhesives according to the stencil design. The open time of the applied

glue is recommended less than 4 hours to avoid over-staging which result to the hardening or "self-curing" property. In this case, the silicon cannot be bonded to the wet adhesives to over-staged adhesives.

The bonded silicon die will be put to the wet adhesives using die-attach process. The thickness of the silicon die can range from 100 – 300 µm. Afterwards, the die bonded units are subjected to oven curing process to create thermo-settlement of the adhesives. In deriving with the applicable adhesive candidate, it is recommended to use sintering glue or highly-filled conductive glue. This is to promote good intermetallic connection for the wire during thermo-compression bonding as seen in Fig 6.

The recommended bondable area or the effective area for intermetallic bonding is 80 – 90%. Micro-porosity of the glue or small amounts of voids visible on the formation of silver intermetallic affect the condition of wire.

Wire bonded samples will be encapsulated with mold compound to incorporate protection to the active silicon die and wiring. Detaching of the stainless carrier can only be done after molding process since the unit will be intact then the unit can be transferred to a tape for the singulation or the cutting to individual unit.

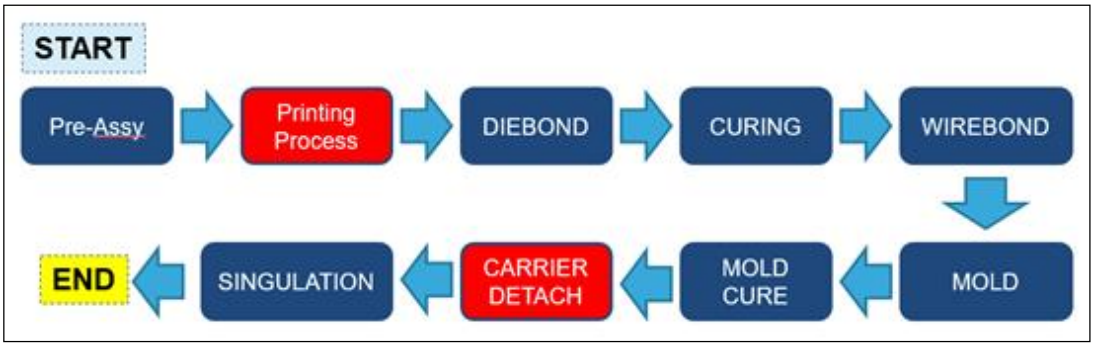


**Fig. 1. Assembly process flow**

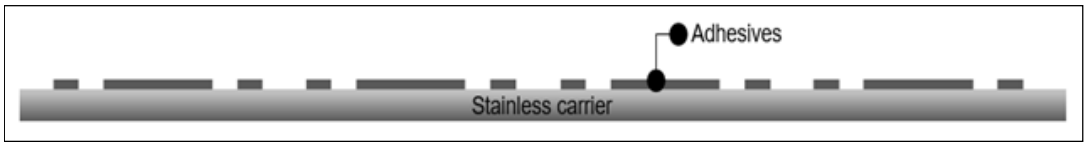


**Fig. 2. Cross-sectional view of adhesives and stainless carrier**

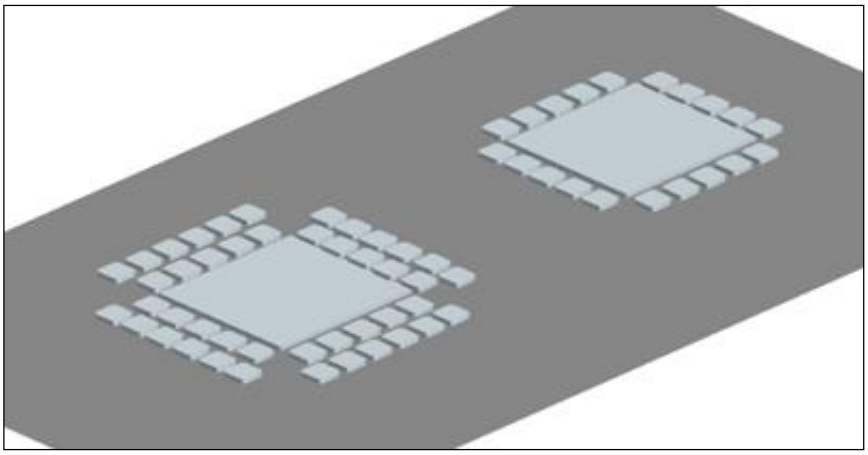

**Fig. 3. Illustration of different I/O design – (left) multiple array I/O; (right) single array**

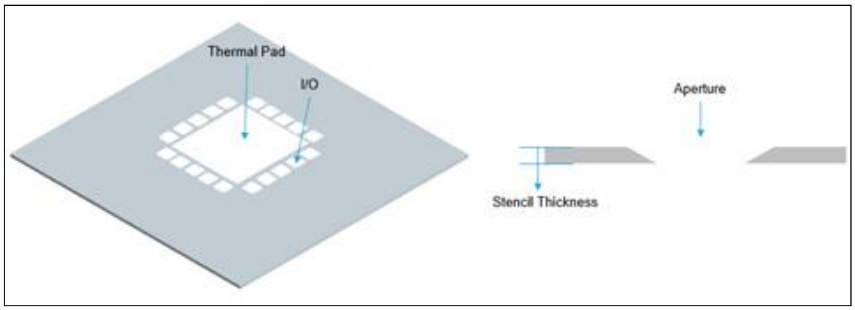


**Fig. 4. Stencil design**

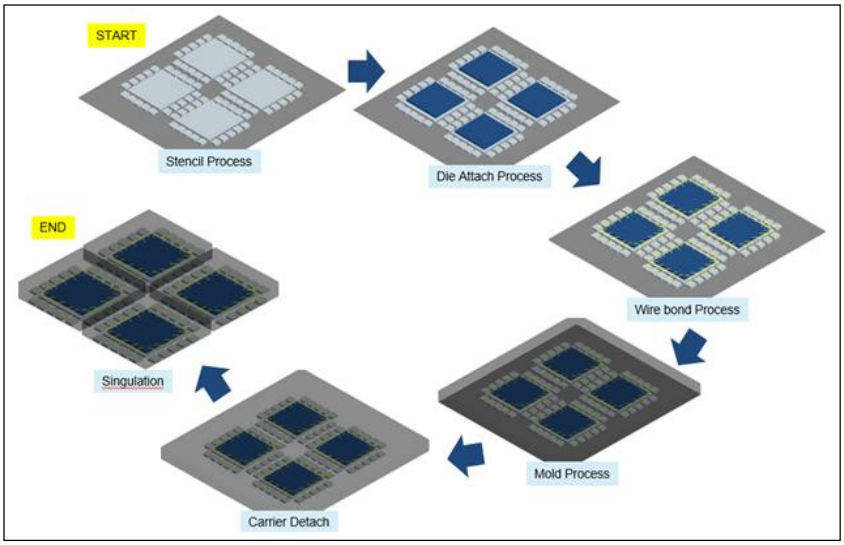


**Fig. 5. Augmented process flow**

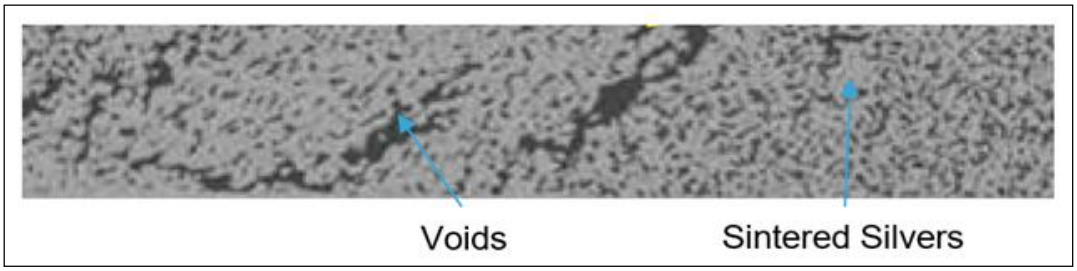


**Fig. 6. Microscopic view of inter metallic connection**

## 3. CONCLUSION

The application of specialized package development promotes multiple advantages from existing surface mount technology. Thinner package is possible using the design concept of the specialized process flow. The design realized the miniaturization of SMT devices wherein multiple I/O can fit inside the proposed package design. The design also offers lower cost due to reusable indirect material and minimal consumption of direct material. Higher thermal and electrical responses could also be achieved due to thinner I/O junction as also discussed in [8].

Prototypes are helpful for future works to validate the effectiveness of the specialized technique of

assembly manufacturing. Though the paper focused on the semiconductor design through the innovative concept of advanced assembly process flow, continuous process improvement is important to foster and sustain high quality performance of assembly manufacturing. Discussions and learnings shared in [9-11] are helpful to improve the assembly manufacturing processes.

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## DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

## COMPETING INTERESTS

Authors have declared that no competing interests exist.

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