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Off-centered Ball Resolution Through Multi-hole Process Plate Implementation at Wirebond Process

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

With the continuous trend of new technologies in semiconductor manufacturing assembly, challenges and issues are unavoidable. This paper presents the modification and improvement done on the process plate design to eliminate the bouncing effect of the silicon die that leads to off-centered ball (OCB) reject during the formation of wire on a quad flat no-leads (QFN) device. The panel type single-row process plate cannot totally vacuum the warped leadframe and this is resulting to off-centered ball. Through changing the panel type single-row process plate to panel type multi-hole process will have a strong vacuum sucked underneath the leadframe and eliminates the occurrence of off-centered ball. Future works could use the improved process plate design for devices of similar configuration.

Keywords: Assembly; bond ball; process plate; wirebond.

1. INTRODUCTION

Wirebond is a process under semiconductor assembly wherein it directly attached a semiconductor wire from a silicon die to the substrate or leadframe to create an electrical connection to the printed wiring board (PWB). This technique of connecting the silicon die to the

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input/output (I/O) became popular due to growing demand for compact and smaller integrated circuit (IC) packaging like QFN, quad flat pack (QFP) packages and ball grid array (BGA) devices that have delicate structure of bonding pads. Note that with new and continuous technology trends and state-of-the-art platforms, challenges are inevitable [1-5].

The wire used is usually made either of gold or aluminum, with copper and silver wires added recently in semiconductor assembly manufacturing industry. The typical wires can be attached using thermocompression method. This technique uses heat that is applied to the material to create a material softening synchronized to the application of pressure to mechanically form an intermetallic between two materials (bond pad to wires). Later development for wire bonding introduces ultrasonic principle together with thermocompression method which is mostly recommended for more delicate structure of bonding pads. In this technique, there is less pressure required and the formation of intermetallic structure is driven by the application of ultrasonic to the capillary.

This paper presents a solution to successfully process this type of packaging technology by using a panel type multi-holes process plate. The leadframe or substrate will totally be vacuumed or sucked underneath to have a stable wirebonding. This in turn will eliminate the bouncing effect of the leadframe. Fig. 1 shows the representation of a wirebonding process.

2. REVIEW OF RELATED LITERATURE AND PROBLEM IDENTIFICATION

Assembly process flow for QFN device is shown in Fig. 2 highlighting the assembly process in focus. Important to note that assembly process flow changes with the product and the technology. Also as previously mentioned, new technologies and breakthroughs bring along its many challenges.

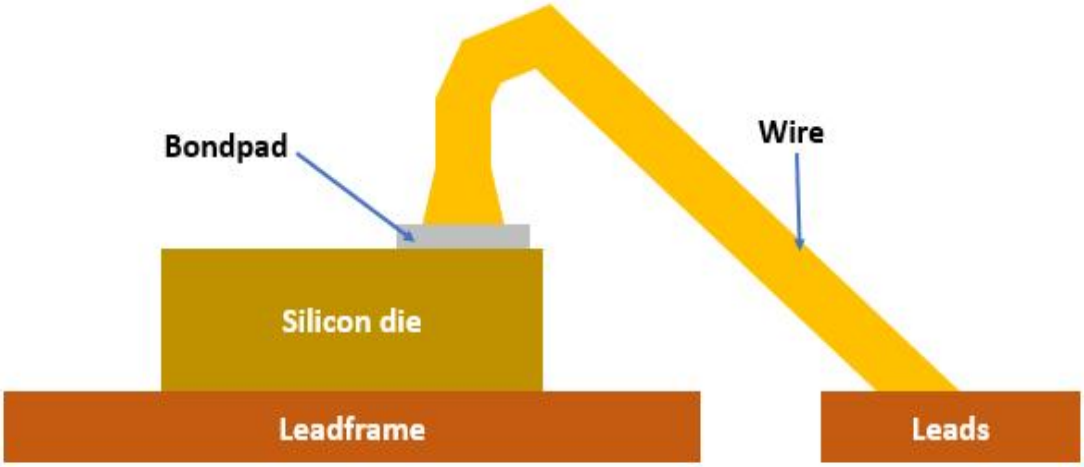

Fig. 1. Wirebonding process

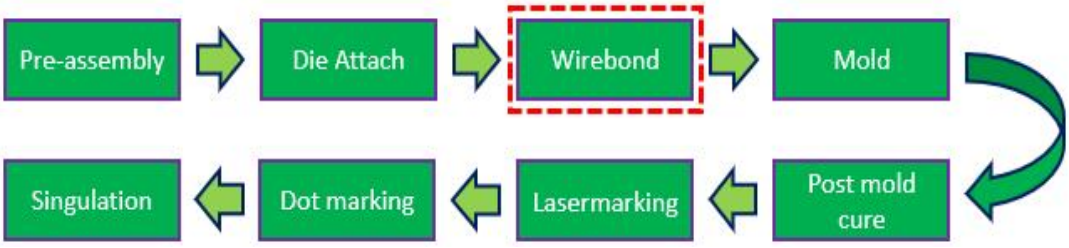

Fig. 2. Actual process flow of QFN

One of the existing defects for wirebonding process is off-centered ball or when the ball is not properly formed a circle on the bond pad. Shown in Fig. 3 is the actual reject manifestation.

An off-centered ball defect may produce bond pad cracks and might damage the internal array

of connection of the silicon die. The manifestation of this defect signifies internal damage that might not be easily detected through series of inspection but greatly affects the functionality of the unit and may failed during the reliability testing of the device.
The application of heat during die attach, oven curing and wirebonding is observed to produce warpage using single-row process plate as shown in Fig. 4. The warpage is mostly contributed to wirebonding process because it has a higher temperature compared to die attach process. The warpage in this study has a significant effect in machine alarm/fallen units from the auto-picker and time-zero (T0) delamination in the mold to leadframe interface.

Fig. 5. shows the actual single-row process plate used in LGA device. The single-row process plate given in Figs. 4 and 5. has a weakness of sucking the leadframe underneath because the warped leadframe are not totally across to the vacuum holes. Another effect of the warped leadframe is bouncing during the attachments of wires. Bouncing effect is observed during the formation of wire for first bond or when the capillary applies force to the silicon die (bonding pad) during the formation of intermetallic between wires.

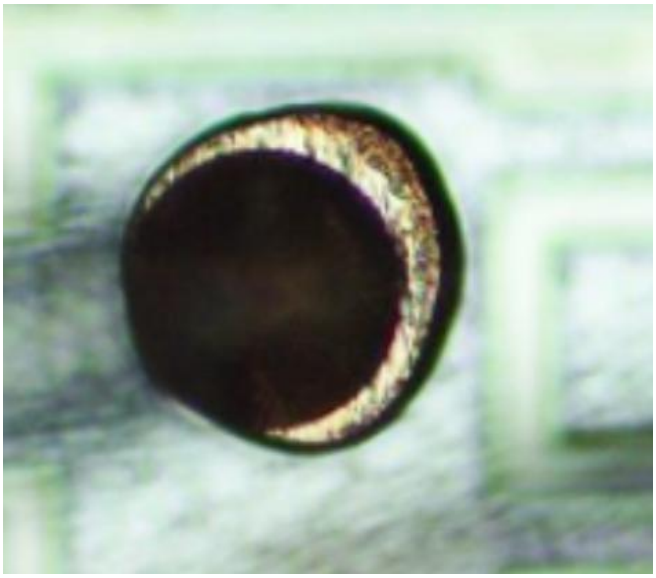

Fig. 3. Actual reject unit

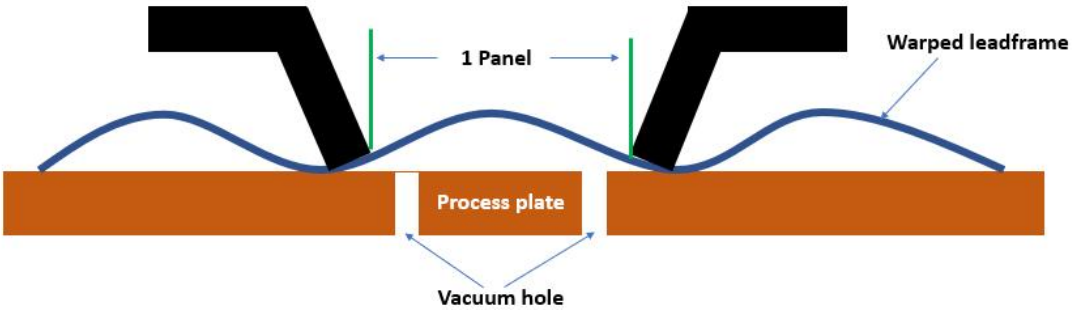

Fig. 4. Warpage illustration using single-row process plate

Fig. 5. Single-row process plate

3. PROCESS AND DESIGN IMPROVEMENT

There are multiple approaches in resolving strip warpage that are known in many assembly sites, however the occurrence of worst warpage in this study is resolved through the improvement and modification of multi-row process plate material. This paper is focused on the optimization of process plate to eliminate the occurrence of off-centered ball through re-designing the vacuum holes of the process plate. A process plate with multi-hole design is shared in Fig. 6. Fig. 7 gives the actual process plate with multi-hole, while Fig. 8 shows a good ball formation when using the said process plate.

The multi-hole applies vacuum underneath the leadframe to the unit that will be wirebonded. This design of process plate is applicable for 1 whole panel depending on the number of rows on the leadframe. This multi-hole design is also relevant to QFN with tape on the backside of the leadframe and QFN tapeless devices.

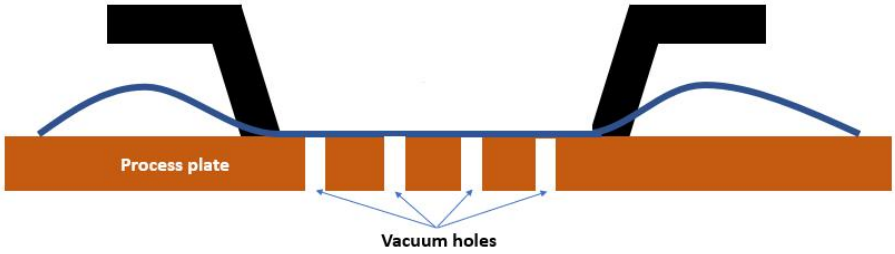

Fig. 6. Process plate with multi-hole design

Fig. 7. Actual process plate with multi-hole

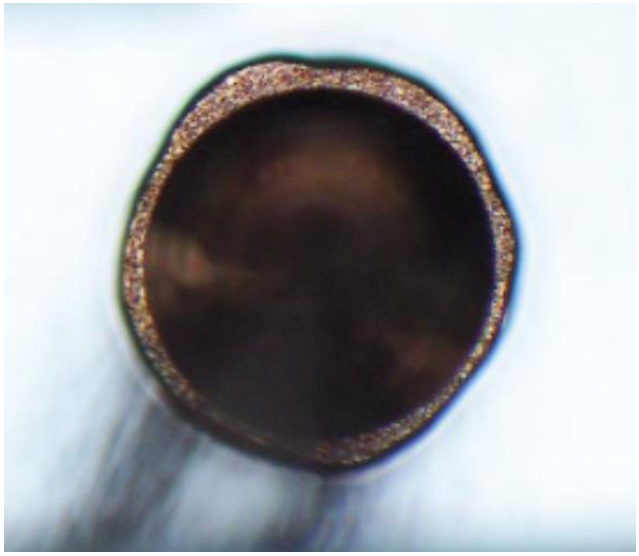

Fig. 8. Actual good ball formation

4. CONCLUSION AND RECOMMENDATIONS

Off-centered ball elimination was successfully realized through the process and design improvement focused on the process plate design. The re-arrangement and introduction of multi-holes on the process design produced a 100% improvement in the off-centered-ball defect reduction with the defect occurrence actually eliminated.

The technique in process plate shared in this study could be used for future works on other semiconductor devices with similar configuration. Comparison of existing works and other studies should also be included for added analysis. Important to note that continuous process improvement is imperative to sustain the high-quality performance of semiconductor products and its assembly manufacturing. Studies and learnings shared in [6-12] are helpful in reinforcing robustness and optimization of assembly processes focused in wirebonding.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT), Malaysia. 2010;1-5.
2. Tan CE, et al. Challenges of ultimate ultra-fine pitch process with gold wire and copper wire in QFN packages. IEEE 36th International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2014;1-5.
3. Sumagpang Jr. A, Rada A. A systematic approach in optimizing critical processes of high density and high complexity new scalable device in MAT29 risk production using state-of-the-art platforms. Presented at the 22nd ASEMEP Technical Symposium. Philippines; 2012.
4. Greig WJ. Integrated circuit packaging, assembly and interconnections. 1st ed. USA: Springer; 2007.
5. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
6. Moreno A, et al. Enhanced loop height optimization for complex configuration on QFN device. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;182-184.
7. Tran TA, et al. Fine pitch probing and wirebonding and reliability of aluminum

capped copper bond pads. IEEE 50th Electronic Components and Technology Conference (ECTC). USA. 2000;1674-1680.
8. Rodriguez R, et al. Implementing single-row process plate design for pre-encapsulated leadframe. Journal of Engineering Research and Reports. 2020;16(2):26-30.
9. Hong SJ, et al. The behavior of FAB (free air ball) and HAZ (heat affected zone) in fine gold wire. Advances in Electronic Materials and Packaging 2001 (Cat. No.01EX506). South Korea. 2001;52-55.
10. Pulido J, Gomez FR. Enhanced wirebonding technique on QFN device with critical die reference. Journal of Engineering Research and Reports. 2021;20(3);57-61.
11. Sameoto D, et al. Wirebonding characterization and optimization on thick film su-8 mems structures and actuators. TRANSDUCERS 2007 - 2007 International Solid-State Sensors, Actuators and Microsystems Conference. France. 2007; 2055-2058.
12. Sumagpang Jr. A, et al. Introduction of reverse pyramid configuration with package construction characterization for die tilt resolution of highly sensitive multi-stacked dice sensor device. IEEE 22nd Electronics Packaging Technology Conference (EPTC). Singapore. 2020;140-146.

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