



# **Wire Shorting Elimination through Wirebond Process Optimization of Semiconductor Sensor Device**

**Anthony Moreno<sup>1\*</sup>, Edwin Graycochea Jr.<sup>1</sup> and Frederick Ray Gomez<sup>1</sup>**

<sup>1</sup>*New Product Development and Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.*

## **Authors' contributions**

*This work was carried out in collaboration among all authors. All authors read, reviewed and approved the final manuscript.*

## **Article Information**

DOI: 10.9734/JERR/2020/v13i417108

### Editor(s):

(1) Dr. Guang Yih Sheu, Chang-Jung Christian University, Taiwan.

### Reviewers:

(1) I. Rexiline Sheeba, Sathyabama Institute of Science and Technology, India.

(2) Josephine Ying Chyi Liew, Universiti Putra Malaysia, Malaysia.

(3) Suman De, SAP Labs India Pvt. Ltd., India.

Complete Peer review History: <http://www.sdiarticle4.com/review-history/57834>

**Received 06 April 2020**

**Accepted 13 June 2020**

**Published 22 June 2020**

**Original Research Article**

## **ABSTRACT**

New and upcoming semiconductor devices and technologies are getting more challenging in assembly manufacturing process due to many factors such as complex package layout, process capability and critical bill of materials. This paper focused on the mitigation of the top major assembly reject of a semiconductor sensor device, that is the wire-to-wire shorting issue at wirebonding process. Parameter optimization particularly the looping segment 1 parameter, as well as using a reverse stitch on ball (RSOB) were employed to eliminate the wire-to-wire defect in wirebonding process. Finally, with the process optimization and improvement, a reduction of 98 percent wire-to-wire shorting occurrence was attained.

**Keywords:** *Wirebonding; wire-to-wire short; process improvement; semiconductor; assembly.*

## **1. INTRODUCTION**

Wirebonding is one of the challenging processes in semiconductor industry for integrated circuit

(IC) assembly. Wirebonding process is responsible in attaching the wires to provide electrical connections through combination of heat, pressure and thermosonic energy. The

\*Corresponding author: Email: [anthony.moreno@st.com](mailto:anthony.moreno@st.com);

design of wirebonding layout of wires in semiconductor sensor device is a very big challenge to process in this type of new technology in wirebond. Note that with new and continuous technology trends and state-of-the-art platforms, challenges are inevitable [1-3]. This paper presents a solution to process this type of new technology with complex wire bonding layout in IC assembly manufacturing by parameter optimization and using a reverse stitch on ball (RSOB). The RSOB has a specific bondpad specially on the pad that wires were short. Reverse stitch on ball means, the process of two-step in one cycle, first is to form a ball bump into the bondpad and then a reverse bonding or the ball bond is bonded into the substrate and stitch on top of the ball bump. To guarantee its integrity during processing, wirebond process is incorporated with a multiple of criteria such as ball size, ball height, ball aspect ratio (BAR), wire pull test, ball shear test, stitch pull test, loop height, intermetallic coverage (IMC) and contact angle. This wirebond criteria is performed after machine conversion or set-up to

ensure the product is reliable when loaded to a reliability test. Fig. 1 shows the actual wire-to-wire shorting defect on a tight wirebonding layout. Criteria for wirebonding are governed by assembly design rules and standard operating procedure [4-5].

## 2. LITERATURE REVIEW AND PROBLEM IDENTIFICATION

A complete assembly process flow for the device in focus starting from pre-assembly to singulation is illustrated in Fig. 2. Worthy to note that assembly manufacturing processes vary with the technology and the product [6-8].

Wire-to-wire shorting is the top major assembly reject in wirebonding process and this was seen during lot processing of the package. This wire-to-wire shorting is caused by capillary that hits the neighboring wire during attaching of wires. The wire used in this package is usually gold or copper with a diameter of less than 1 millimeter. One of the most challenging method in



Fig. 1. Wire-to-wire shorting defect

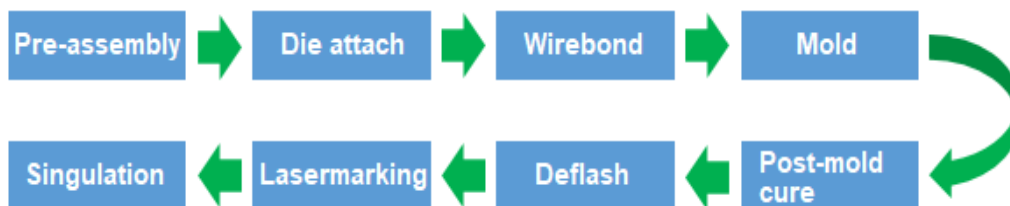


Fig. 2. Assembly process flow

wirebonding is to eliminate the wire-to-wire shorting issue. During looping process, parameter optimization is normally done in this type of technology, but the parameter is not yet enough to solve the issue encounter on this package. Optimization of wire looping is very challenging because the wiring layout has a very tight configuration and this could affect the whole package when subjected to reliability.

### 3. PROCESS DEVELOPMENT SOLUTION AND DISCUSSION OF RESULTS

An improved and enhanced process solution in wirebonding is comprehensively done with the combination of wire looping parameter optimization and by RSOB method. Fig. 3 shows the RSOB actual cycle eliminating the wire-to-wire shorting issue. With that reverse stitch on ball and parameter optimization, no wire-to-wire shorting occurrence seen after implementing this improvement in wirebonding process. Looping segment 1 parameter is adjusted and optimize to solve the problem of wire-to-wire shorting. Segment 1 parameter means

that during looping, the wire will bend to the left to prevent not touching the neighboring wire. With this parameter, the package is already in mass production. Fig. 4 illustrates the response of segment 1 parameter, while Fig. 5 shares the actual unit with no wire shorting issue using the optimized parameter and RSOB method. One of the advantages of the solution is the unit per hour (UPH) is increased and this is a good achievement to make the delivery of units will move firm as well. The optimized looping parameter and RSOB will eventually have a good reliability test on this type of technology.

The optimized loop parameter eventually served as the good loop formation, which also passed the destructive wire-pull test. A medium to large scale of validation was done to see the difference on the improvement done. A 98 percent improvement highlighted in Fig. 6 was achieved for wire-to-wire shorting reduction by implementing this RSOB plus segment 1 parameter. Note that actual parts per million (ppm) numbers are intentionally not shown due to confidentiality.

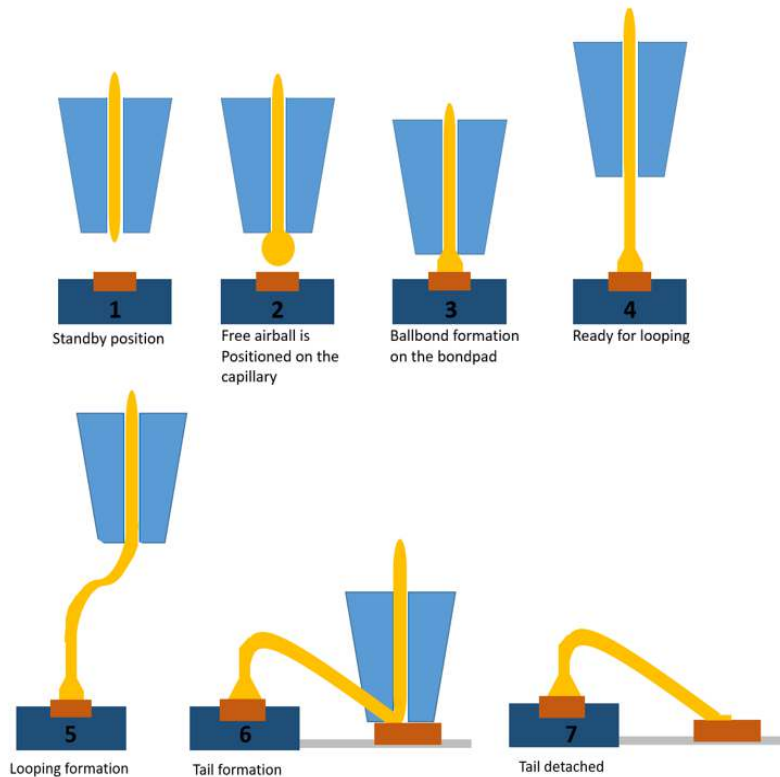


Fig. 3. Reverse stitch on ball actual cycle

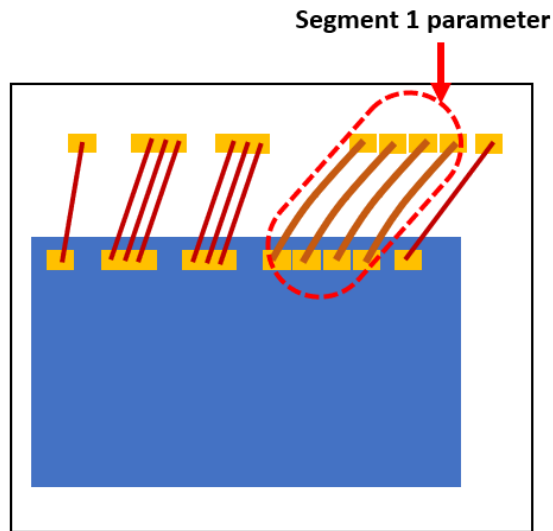


Fig. 4. Response of segment 1 parameter

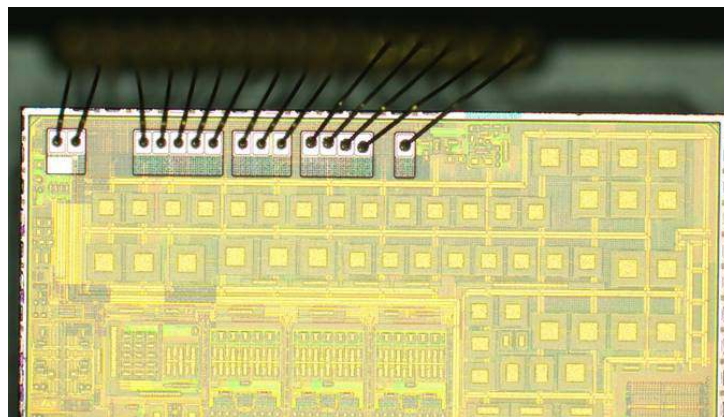


Fig. 5. Actual unit with improved wirebonding and no wire-to-wire shorting

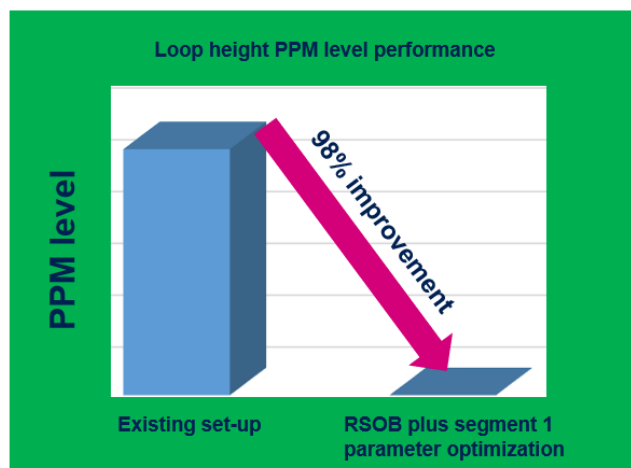


Fig. 6. Defect ppm level performance improvement

#### 4. CONCLUSION AND RECOMMENDATIONS

With the complete wirebond process optimization and characterization particularly on the looping segment 1 parameter, wire looping resolution was successfully achieved for this type of new technology in semiconductor industry with tight wiring layout. The improved solution is considered a key milestone which could be used for future reference in all semiconductor industry with similar wiring layout construction. Worth noting is that continuous process and design improvement is really important to sustain the high quality performance of semiconductor products and their assembly manufacturing. Works in [9-10] are helpful in reinforcing robustness and optimization of assembly processes particular at wirebonding process.

#### ACKNOWLEDGEMENT

The authors would like to thank the New Product Development & Introduction (NPD-I) team and the Management Team (MT) for the continuous support.

#### COMPETING INTERESTS

Authors have declared that no competing interests exist.

#### REFERENCES

1. Tan CE, Liong JY, Dimatira J, Tan J, Kok LW. Challenges of ultimate ultra-fine pitch process with gold wire & copper wire in QFN packages. 36<sup>th</sup> International Electronics Manufacturing Technology Conference, Malaysia; 2014.
2. Liu Y, Irving S, Luk T, Kinzer D. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; 2008.
3. Lall P, Deshpande S, Nguyen L. Reliability of copper, gold, silver and PCC wirebonds subjected to harsh environment. IEEE 68<sup>th</sup> Electronic Components and Technology Conference, San Diego, California, USA; 2018.
4. STMicroelectronics. Assembly and EWS design rules for wire bond interconnect dice. rev. 54; 2019.
5. STMicroelectronics. Au wire for thermocompression ultrasonic and thermosonic wire bonding operation. rev. 61; 2019.
6. Harper C. Electronic packaging and interconnection handbook. 4<sup>th</sup> ed., McGraw-Hill Education, USA; 2004.
7. Geng H. Semiconductor manufacturing handbook. 2<sup>nd</sup> ed., McGraw-Hill Education, USA; 2017.
8. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1<sup>st</sup> ed., Wiley-IEEE Press, USA; 2006.
9. Sumagpang Jr. A, Graycochea Jr. E, Gomez FR. Package design improvement for wire shorting resolution. Journal of Engineering Research and Reports. 2020; 11(2):41-44.
10. Pulido J, Gomez FR, Graycochea Jr. E. Wirebond process improvement with enhanced stand-off bias wire clamp and top plate. Journal of Engineering Research and Reports. 2020;9(3):1-4.

© 2020 Moreno et al.; This is an Open Access article distributed under the terms of the Creative Commons Attribution License (<http://creativecommons.org/licenses/by/4.0>), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly cited.

Peer-review history:

The peer review history for this paper can be accessed here:  
<http://www.sdiarticle4.com/review-history/57834>